MONOLITHIC FREQUENCY DOUBLERS

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ABSTRACT

Monolithic frequency doublers have been fabricated and tested. Planar Schottky barrier varactor diodes, RF matching circuits and bias lines are integrated on a 4 mm by 8 mm GaAs substrate, demonstrating the feasibility of monolithic frequency multipliers for the first time.

Output powers greater that 20 mW are obtained from 25.6 to 27.4 GHz. In this frequency range maximum output powers are ~43 mW with conversion efficiences of ~20%. Maximum efficiencies of 24% are obtained at a reduced output power of 25 mW.

INTRODUCTION

Varactor diode frequency multipliers have been widely used as sources of microwave and millimeter-wave power and have been built with performance parameters covering a wide range of output frequency, power and conversion efficiency. In addition, theoretical performance limits have been studied extensively.[1,2] These analyses show that RF performance depends primarily upon the cut-off frequency of the varactor diode and the quality factor of the RF circuit. The cut-off frequency is influenced by the device design, and the circuit quality factor is related to the particular circuit and its implementation. At the present time monolithic circuits are of particular interest because of their potential for low-cost fabrication and small-size realization. In addition, monolithic fabrication is inherently capable of producing large numbers of identical devices which may be combined effectively to increase output power.

Prior work in GaAs monolithic microwave integrated circuits (MMICs) using passive two-terminal devices has been devoted to the integration of mixer diodes in monolithic mixers[3,4,5,6] and monolithic mixer-preamplifiers.[7] An effort towards the integration of monolithic frequency triplers[8] on GaAs took place in the late sixties. However no electrical test results were reported.

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The present paper reports for the first time RF performance data obtained from monolithic frequency doublers in which a planar Schottky barrier varactor diode is integrated in a microstrip circuit on a GaAs substrate. The intended use of this monolithic frequency doubler is for integration into a heterodyne receiver to provide local oscillator power and also as the output stage of a transmitter.

RF CIRCUIT DESIGN

The monolithic frequency doubler was designed with the assistance of scaled models. A 0.63 GHz to 1.26 GHz hybrid prototype is shown in Fig. 1. Near the center of the circuit a packaged varactor diode is attached to input and output matching networks. The zero-bias capacitance of this diode is 5.6 pF. The microstrip lines are fabricated with adhesive copper foil[8] applied to a ceramic substrate.[9] The substrate thickness is 3.95 mm and the dielectric constant is 12.97, similar to that of GaAs. The circuit elements in this prototype can be conveniently modified because the parasitic effects of diode packages and wires are negligible at low frequencies. This is in contrast to modifications in the actual monolithic circuit which require the generation of new masks and the processing of new devices and circuits. Such operations are both expensive and time consuming.

Also shown in Fig. 1 is the GaAs monolithic frequency doubler, which was designed by scaling down the dimensions from the lower frequency prototype by a factor of 22.57. The scaled values for the thickness of the GaAs substrate and zero-bias junction capacitance are 0.175 mm and 0.25 pF respectively. Calculated values of scaled input and output frequencies are 14.22 and 28.44 GHz. These calculated values proved somewhat higher than the measured operating frequencies of the monolithic circuit because the junction capacitance of the integrated varactor diode was ~.35 pF, higher than the design value.

The microstrip implementation shown in Fig. 1 was chosen for its simplicity. The series connection of the diode was selected because planar varactor diodes can be fabricated with anode and cathode contacts as integral parts of the transmission lines. Input and output matching networks consist of quarter-wave transformer sections with open circuited shunt stubs which are resonant at

output and input frequencies. Their positions were selected to reflect the appropriate impedances at the plane of the diode.

DEVICE DESIGN AND FABRICATION SEQUENCE

The construction of the planar varactor diode is illustrated in Fig. 2. The anode is formed by a metal-semiconductor Schottky barrier on a ~1 μm thick n-type layer doped to a concentration of ~2 x 10^{16} cm^{-3}. The area of the anode is ~560 μm^2. The cathode is formed on a 3.5 to 4.0 μm thick n^+ layer doped to a impurity concentration in the range of 2 to 3 x 10^{18} cm^{-3}. The cross-hatched areas in Fig. 2 represent regions of GaAs that are rendered semi-insulating by the bombardment of protons. These regions enable the connection of circuit elements to the anode over the etched step of the mesa.

Major operations in the fabrication sequence of the varactor diode doubler are the formation of ohmic contacts, the electrical isolation of devices, the formation of a Schottky barrier anode junction, and the plating of circuit elements, as illustrated by Fig. 3. Fabrication begins with the definition of windows in the photoresist layer for the ohmic contacts. The n-layer is then etched away from these areas, after which the ohmic contact metals are evaporated and the contacts are formed by photoresist lift-off. The contacts are alloyed at 460°C. Specific contact resistances below 10^{-6} Ω cm^2 are usually obtained. The ohmic contact alloyed into the n^+ layer is illustrated in Fig. 3a. The electrical isolation of devices is accomplished in two steps, mesa etching followed by proton bombardment, as illustrated in Fig. 3b. The two step isolation process is used because the combined thickness of the n and n^+ layers is approximately 5.0 μm, which is in excess of the layer thickness that the available 400 keV proton beam can render insulating. The bombardment mask is designed to expose the etched mesa step of the anode to the proton bombardment, enabling the fabrication of the transmission line over the mesa step adjacent to the anode, as shown in Fig. 3c. The anode is formed by an evaporated platinum layer on n-type GaAs. The microstrip lines and bias lines are then electroplated with gold to multiple skin depths as shown in Fig. 3c. The process is completed with a low energy proton implant which is used to passivate the GaAs region between the anode and cathode contacts. A monolithic circuit produced by this process is shown in Fig. 4. The die measures 4 mm by 8 mm. The planar varactor diode is shown at a higher magnification in Fig. 5.

TEST RESULTS

Devices produced by the above process exhibit ideality factors of 1.05 and breakdown voltages of 18 V. The junction capacitance of the diode is plotted as a function of the reverse bias voltage in Fig. 6. The zero bias junction capacitance of 0.35 pF is approximately 0.1 pF higher than the design value. The consequence of this higher capacitance is a shift in the operating frequency of the doubler.

The varactor frequency doubler is mounted in a test fixture between two short sections of 50 Ω microstrip lines fabricated on 0.010" alumina substrates. The microstrip lines are connected to OSSM launchers. The combined RF losses of the launchers and microstrip-lines are estimated conservatively as ~.3 dB at the input and ~.5 dB at the output. The RF test results of the monolithic frequency doubler are shown in Fig. 7 and Fig. 8. The data pertains to measured power levels at the connectors of the test fixture. Performance at the chip level is obtained by accounting for RF losses in the test fixture. The output power as a function of output frequency is plotted in Fig. 7. In this measurement the input power is kept constant at 182.4 mW. Between 25.6 and 27.4 GHz the output power is in excess of 17.5 mW, and the 3 dB output bandwidth is approximately 2 GHz. At the chip level the output power exceeds 20 mW over this frequency range. The relationship of output power and conversion efficiency to input power is shown in Fig. 8. In this measurement the frequency is kept constant at 25.8 GHz. The maximum output power is 38.6 mW at 15.5% efficiency. At the chip level the corresponding maximum output power and conversion efficiency are 43 mW and 20%, respectively. At the chip level a maximum conversion efficiency of 24% is obtained at a reduced output power of 25 mW.

CONCLUSION

A monolithic varactor frequency doubler has been fabricated. The output powers obtained are adequate for use as local oscillators in heterodyne receivers. Since the monolithic varactor fabrication sequence is compatible with monolithic mixer technology, it is possible to fabricate a monolithic balanced mixer which includes a varactor frequency doubler in the local oscillator circuit. Furthermore, because the integration of GaAs FET's and microwave diodes has already been demonstrated,[7] it is possible to incorporate an amplifier to drive the frequency doubler, and a low noise IF amplifier to follow the balanced mixer. Such monolithic heterodyne receivers have important applications in radar and communications systems. For applications where higher output powers are necessary, such as in transmitters, the output power can be increased by optimizing the design of the device and embedding circuit as well as by means of power-combining techniques.

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10. Commercial product D-13 from Trans-Tech, Inc., Gaithersburg, Maryland.

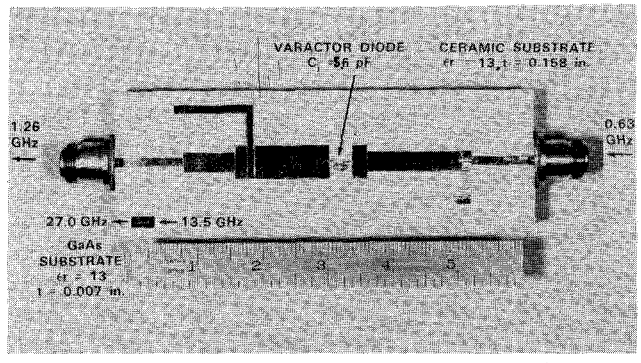

Fig. 1. Scaled model for the design of monolithic frequency doublers. The scaling factor is 22.57 to 1.

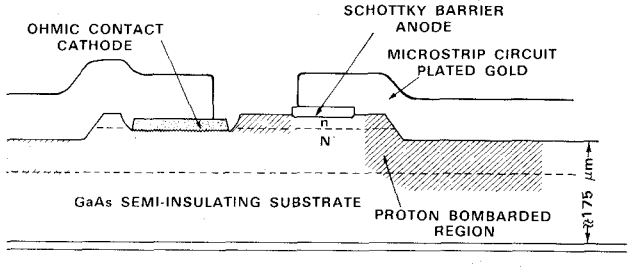

Fig. 2. Planar monolithic varactor diode with n and n^+ epitaxial layers used for the anode and cathode contacts, respectively. The transmission lines are formed over proton bombarded regions.

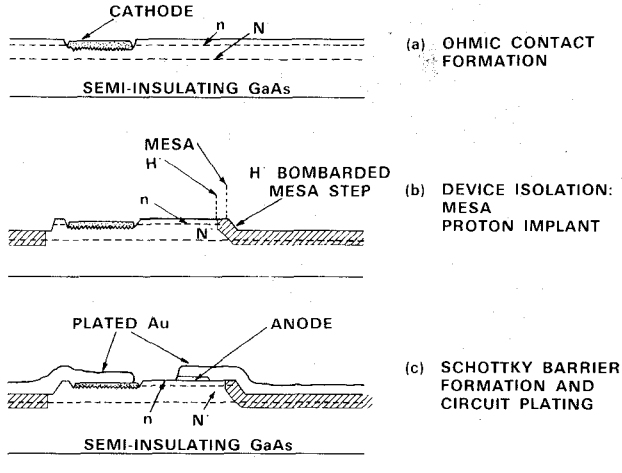

Fig. 3. Highlights of fabrication sequence (a) Ohmic contact formation (b) Device isolation: mesa and proton bombardment (c) Schottky barrier formation and circuit plating.

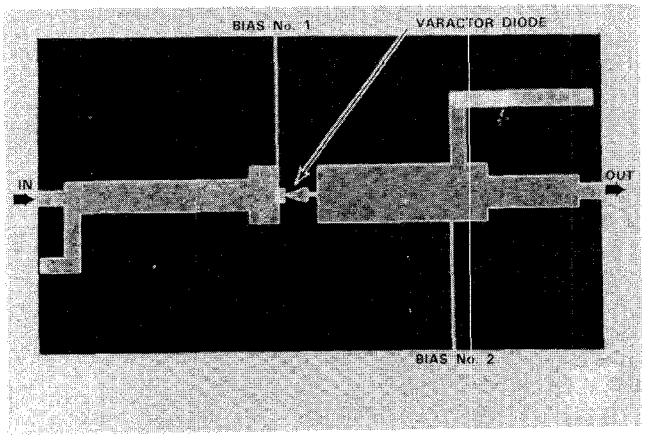

Fig. 4. Monolithic frequency doubler. A varactor diode is integrated with microstripline circuits and bias lines. Dimensions of the chip are 4 mm x 8 mm.

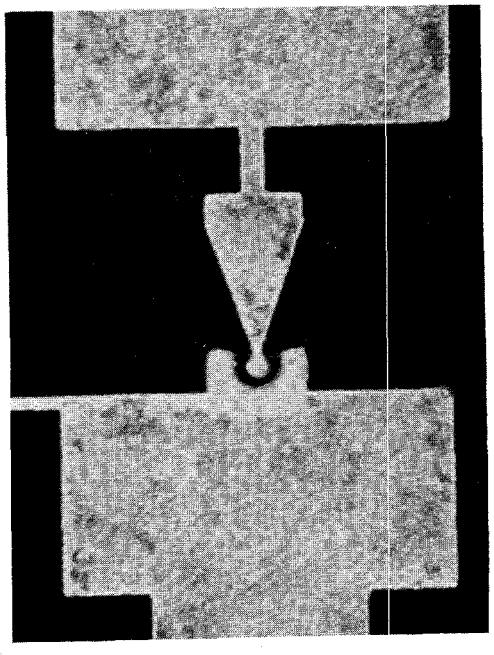

Fig. 5. Monolithic varactor diode. The diode terminals are an integral part of the embedding circuit.

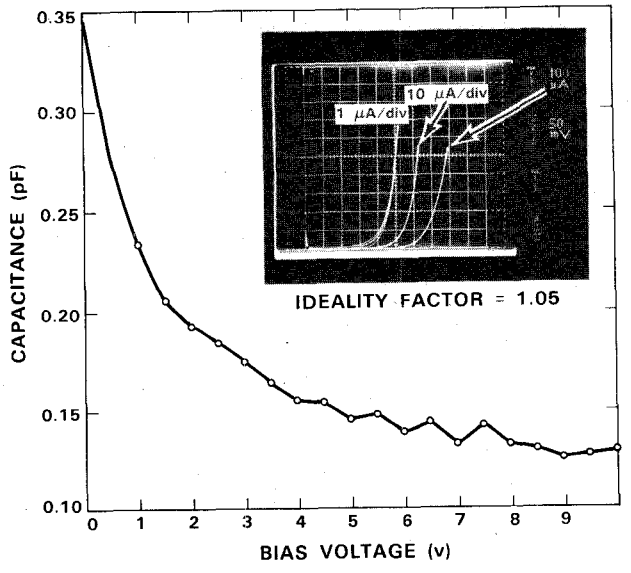

Fig. 6. Junction capacitance vs. reverse bias voltage of monolithic varactor diode. The inset shows forward diode currents vs. bias voltage in a multiple exposure photograph. The traces correspond to three current scales: 1 μA/div, 10 μA/div and 100 μA/div.

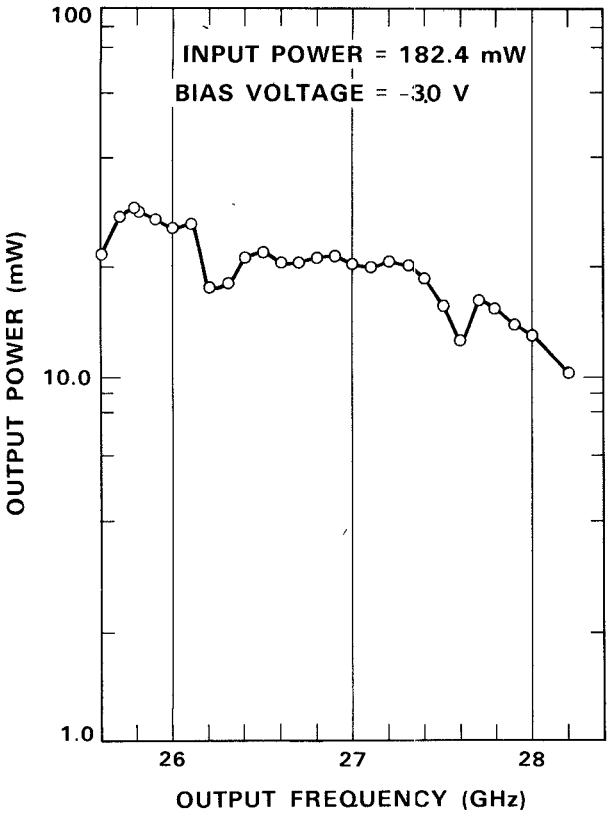

Fig. 7. Output power vs. output frequency curve of monolithic varactor frequency doubler at test fixture terminals.

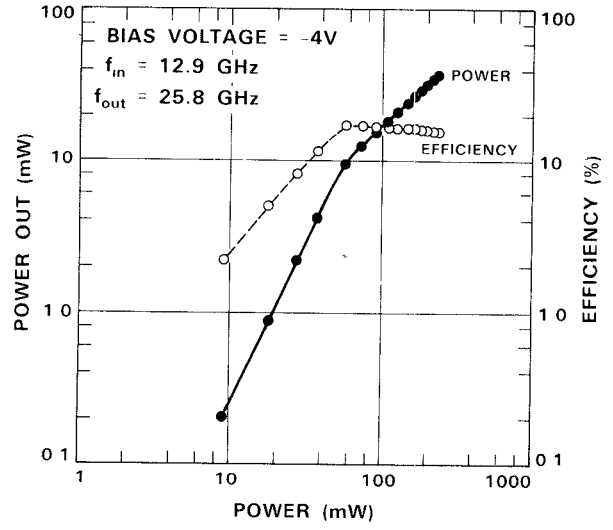

Fig. 8. Measured output power and conversion efficiency of monolithic varactor frequency doubler as a function of input power at test fixture terminals.